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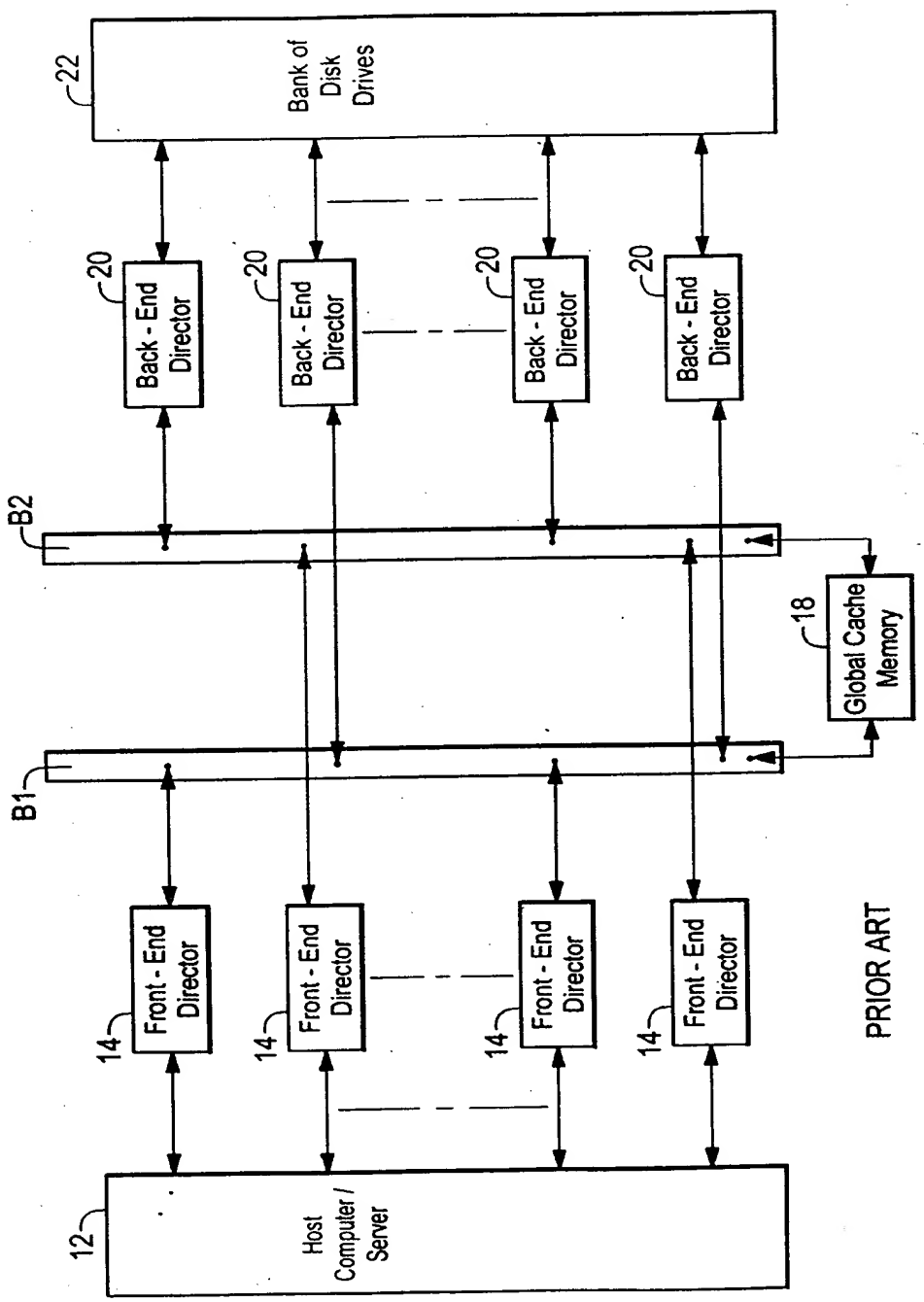

PRIOR ART

FIG. 1

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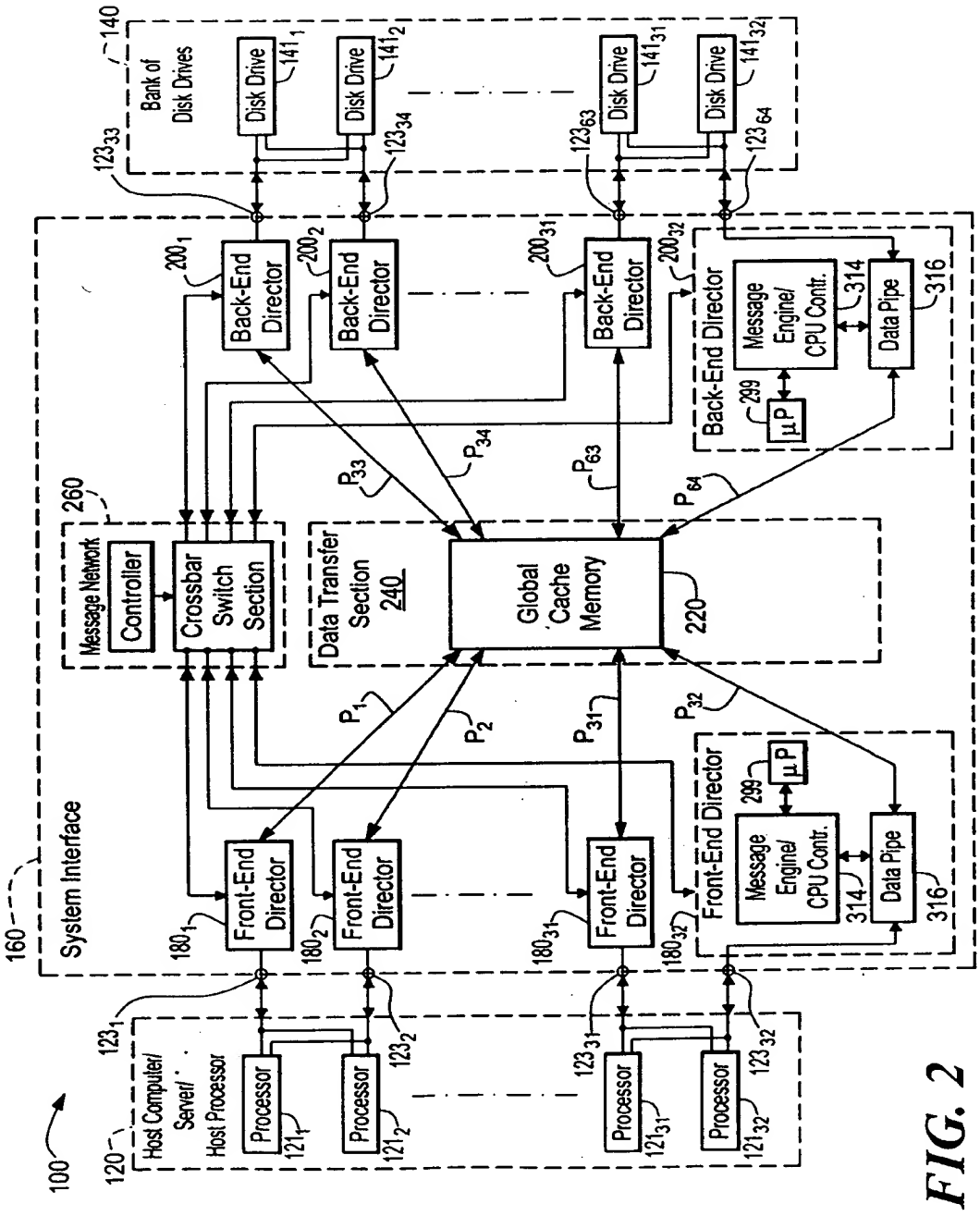
100
120
Host Computer/ Server/ Host Processor
Processor
121
123
160
System Interface
180
Front-End Director
Front-End Director
Front-End Director
Front-End Director
Message Engine/ CPU Contr.
299
µP
314
Data Pipe
316
Front-End Director
Message Engine/ CPU Contr.
299
µP
314
Data Pipe
316
Back-End Director
Back-End Director
Back-End Director
Back-End Director
200
Message Network
260
Controller
Crossbar Switch Section
Data Transfer Section 240
Global Cache Memory
220
P1
P2
P31
P32
P33
P34
P63
P64
Bank of Disk Drives
140
Disk Drive
141
123

FIG. 2

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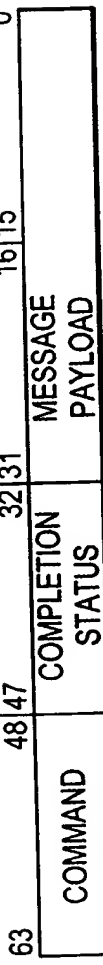

FIG. 2A

FIG. 2B

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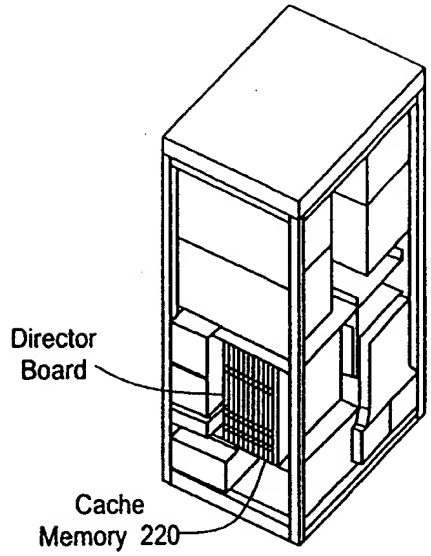

FIG. 3

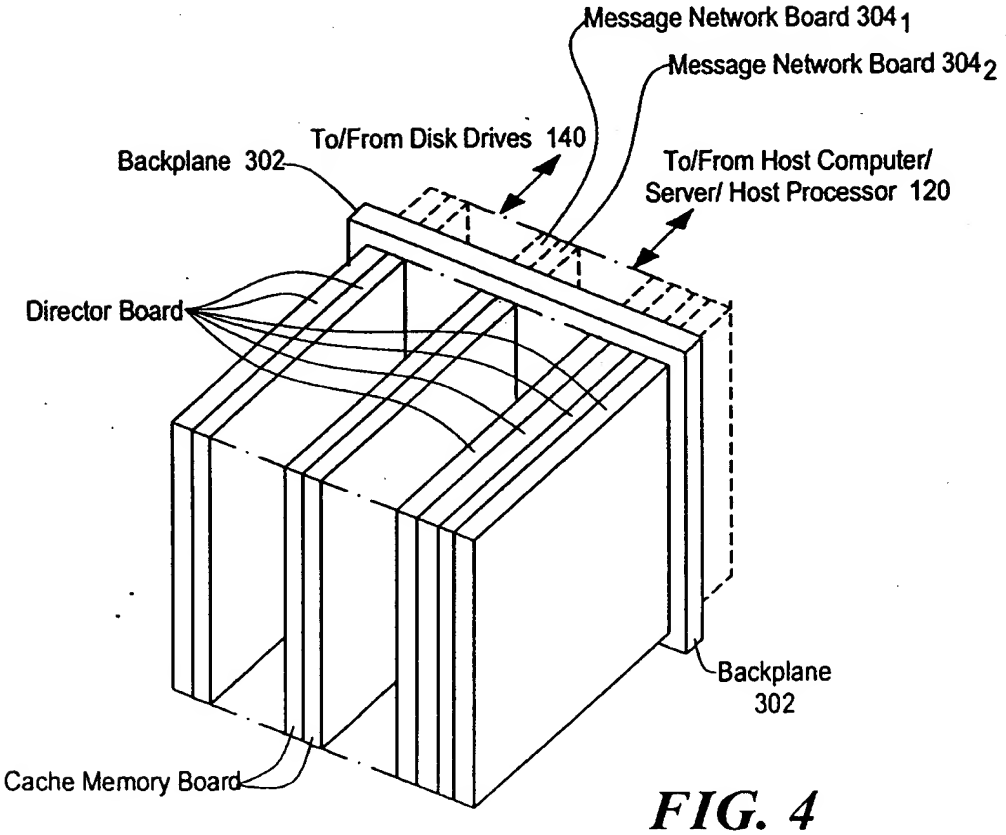

FIG. 4

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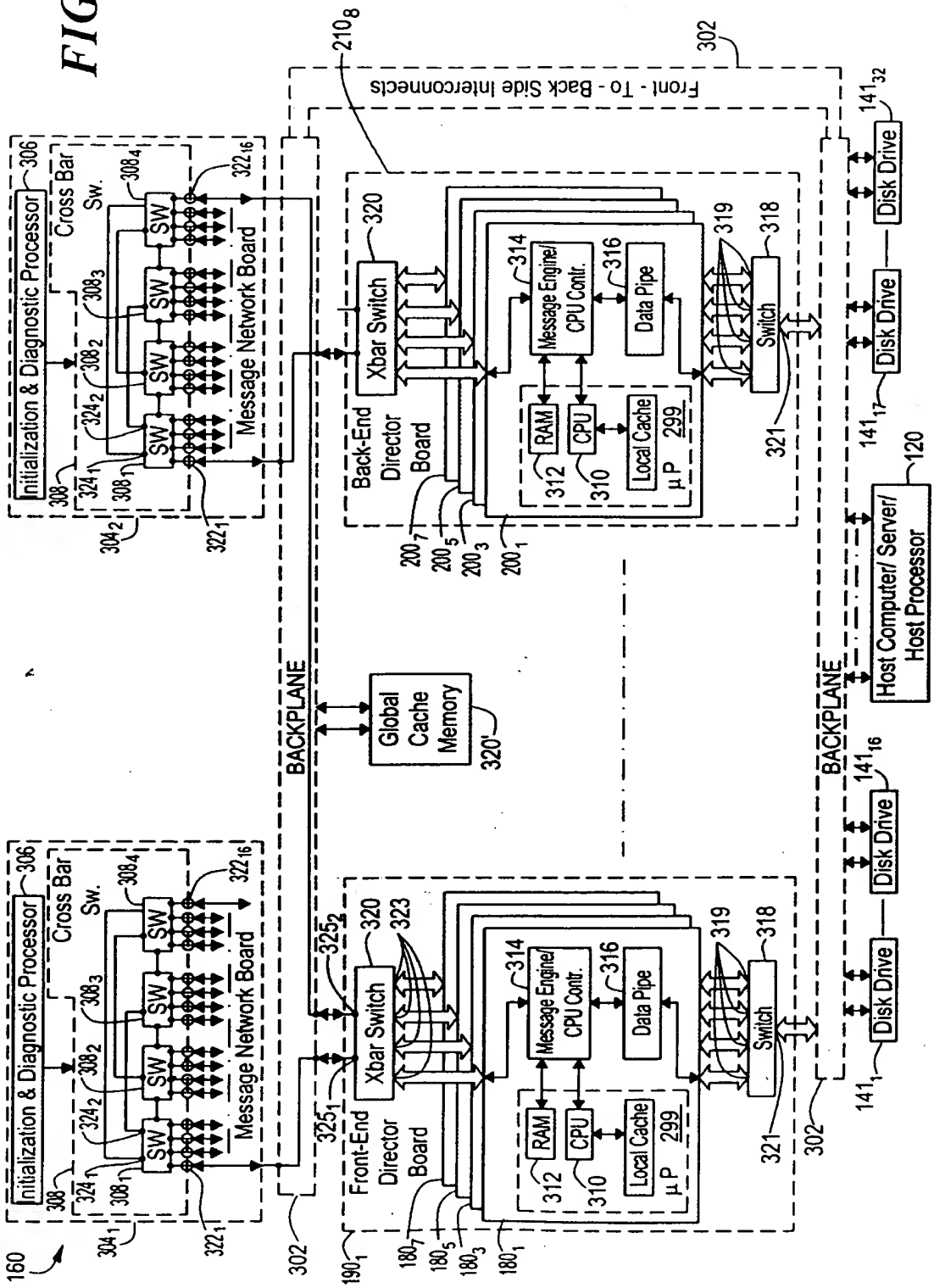
FIG. 5


Front - To - Back Side Interconnects
Initialization & Diagnostic Processor
Cross Bar Sw.
Message Network Board
Back-End Director Board
Front-End Director Board
Xbar Switch
Message Engine/ CPU Contr.
Data Pipe
Switch
RAM
CPU
Local Cache µP
BACKPLANE
Global Cache Memory
Host Computer/ Server/ Host Processor
Disk Drive

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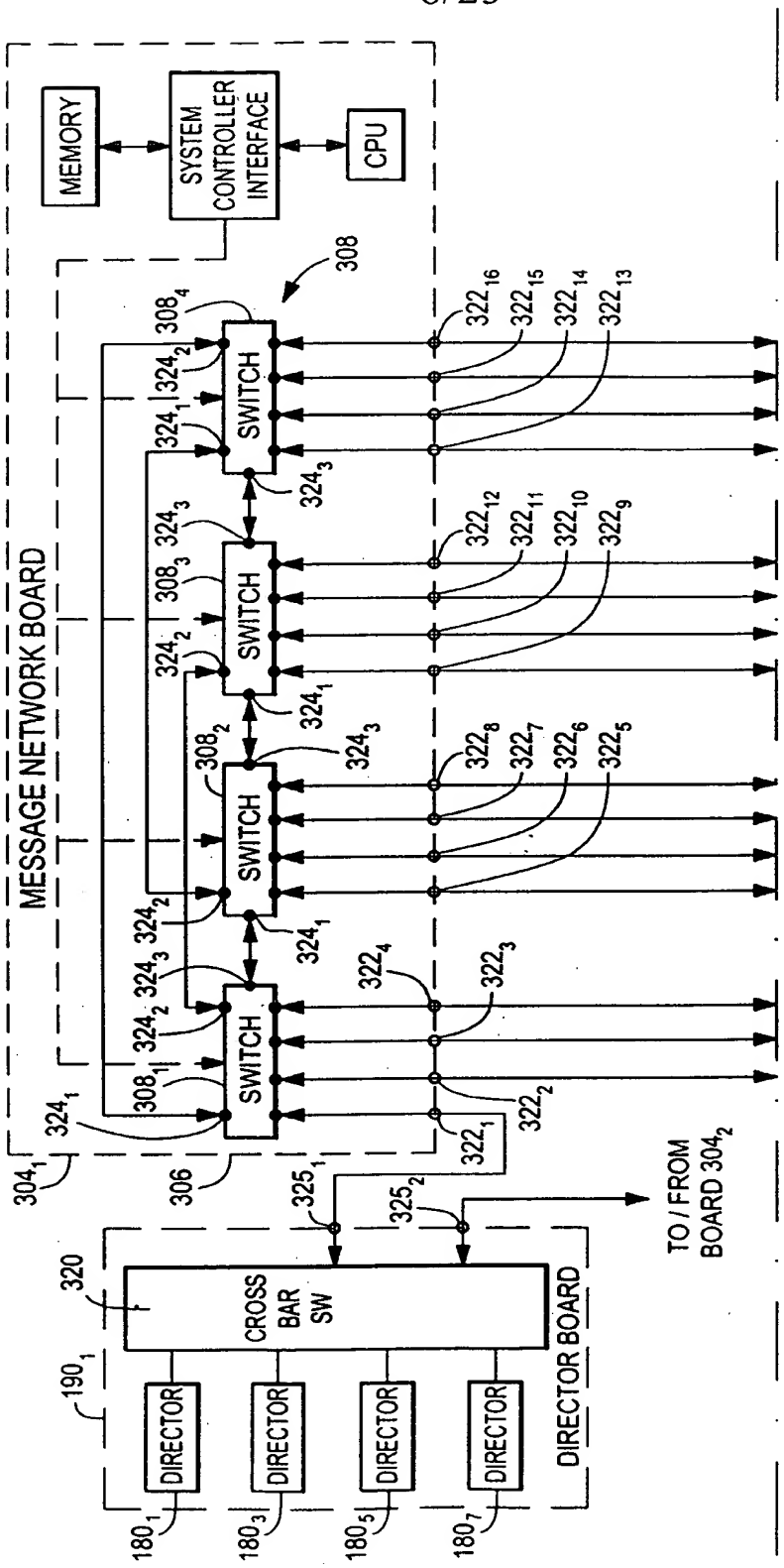

FIG. 6A

FIG. 6

FIG. 6A
FIG. 6B

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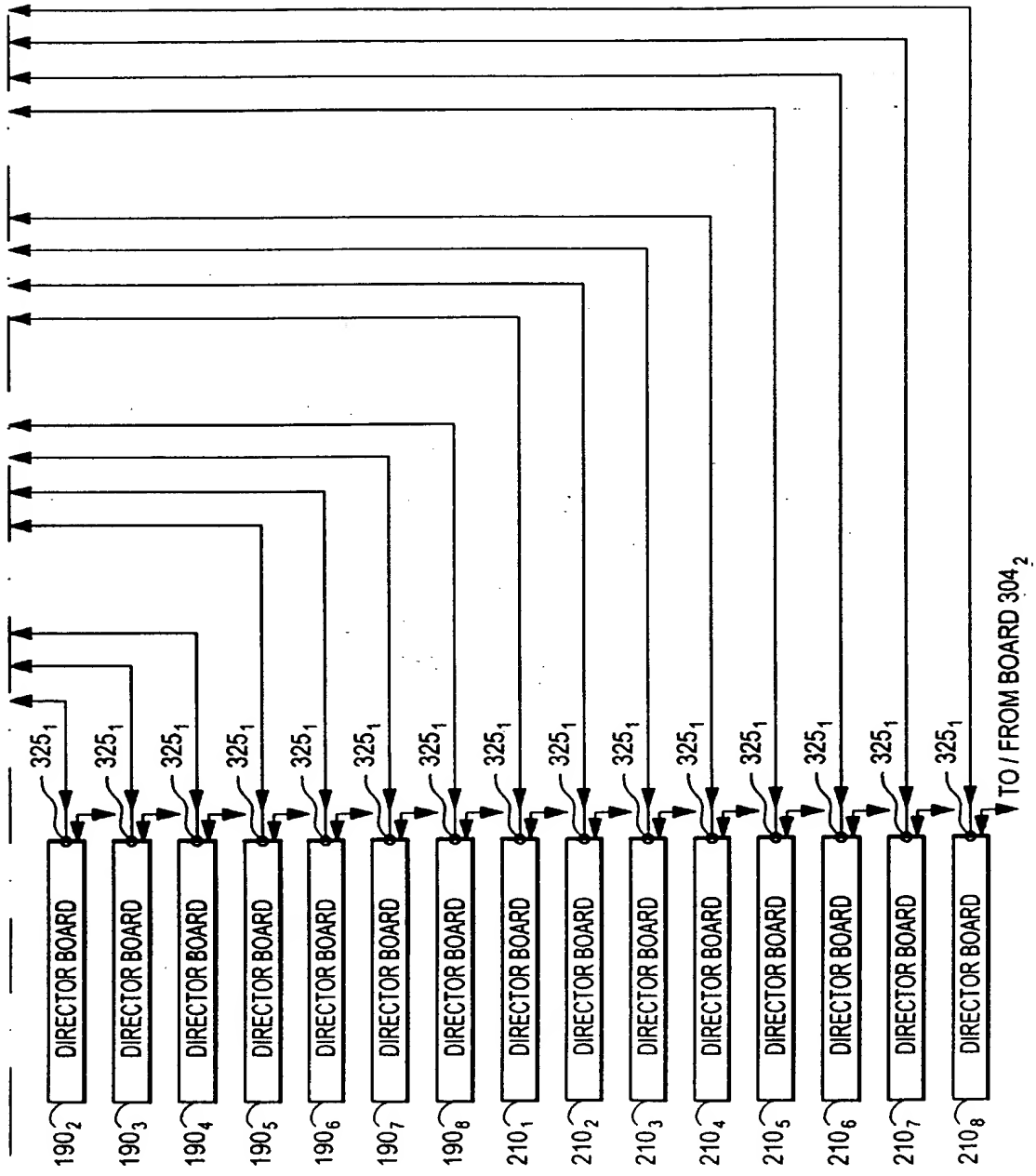
FIG. 6B


FROM FIG. 6A
DIRECTOR BOARD
190_2
190_3
190_4
190_5
190_6
190_7
190_8
210_1
210_2
210_3
210_4
210_5
210_6
210_7
210_8
325_1
TO / FROM BOARD 304_2

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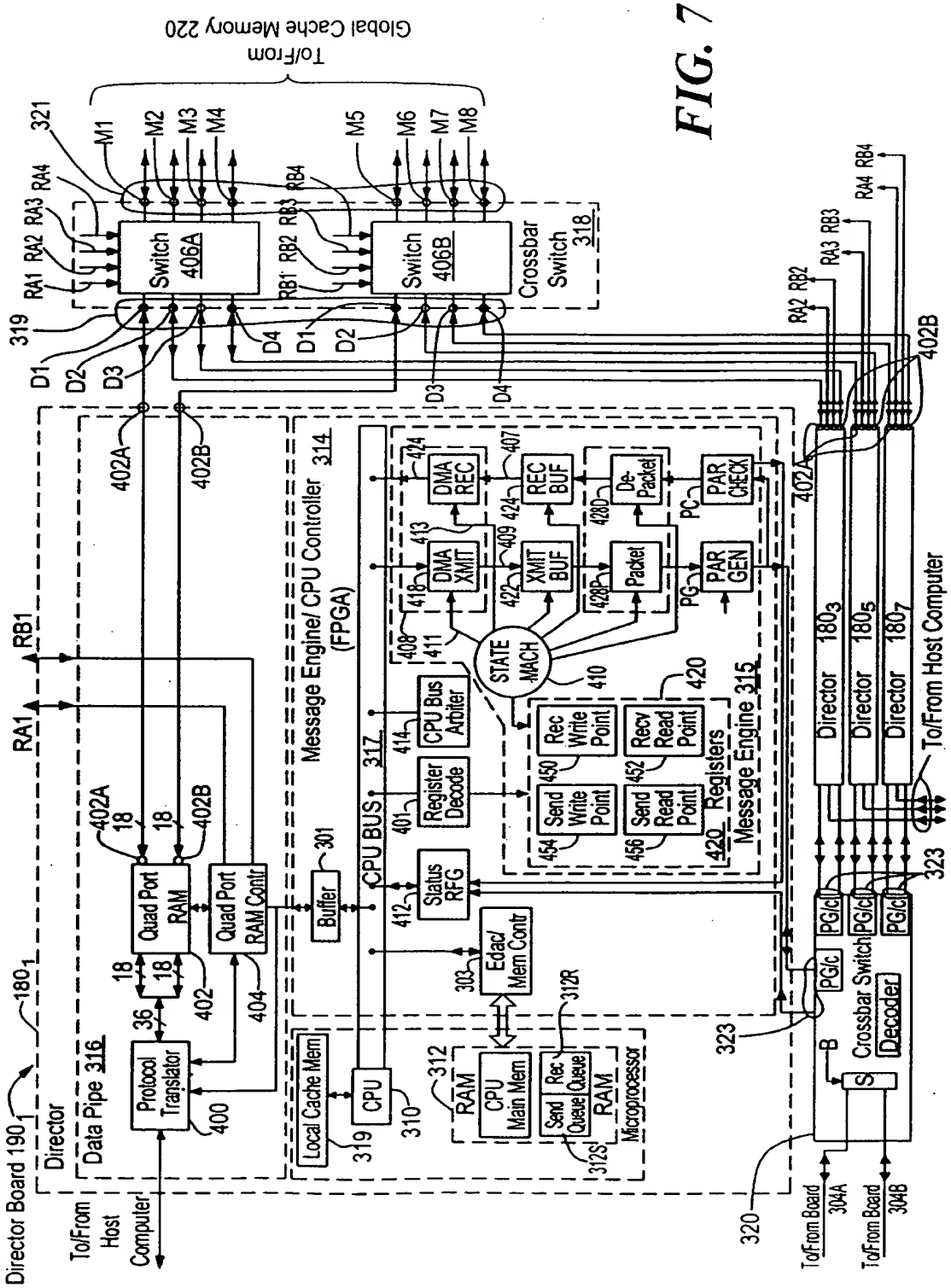
To/From Global Cache Memory 220
M1
M2
M3
M4
M5
M6
M7
M8
321
RA1
RA2
RA3
RA4
RB1
RB2
RB3
RB4
Switch 406A
Switch 406B
Crossbar Switch 318
319
D1
D2
D3
D4
402A
402B
Message Engine/ CPU Controller 314 (FPGA)
DMA REC
REC BUF
De-Packet
PAR CHECK
DMA XMIT
XMIT BUF
Packet
PAR GEN
STATE MACH
CPU Bus Arbiter
Register Decode
Rec Write Point
Recv Read Point
Send Write Point
Send Read Point
Message Engine 315 Registers
CPU BUS 317
Status RFG
Edac/ Mem Contr
Buffer
Quad Port RAM
Quad Port RAM Contr
Director Board 190 1
Director
Data Pipe 316
Protocol Translator
Local Cache Mem
CPU
CPU Main Mem
Send Rec Queue Queue
RAM
Microprocessor
To/From Host Computer
Director 180 3
Director 180 5
Director 180 7
To/From Host Computer
PG/c
Crossbar Switch
Decoder
To/from Board 304A
To/from Board 304B

FIG. 7

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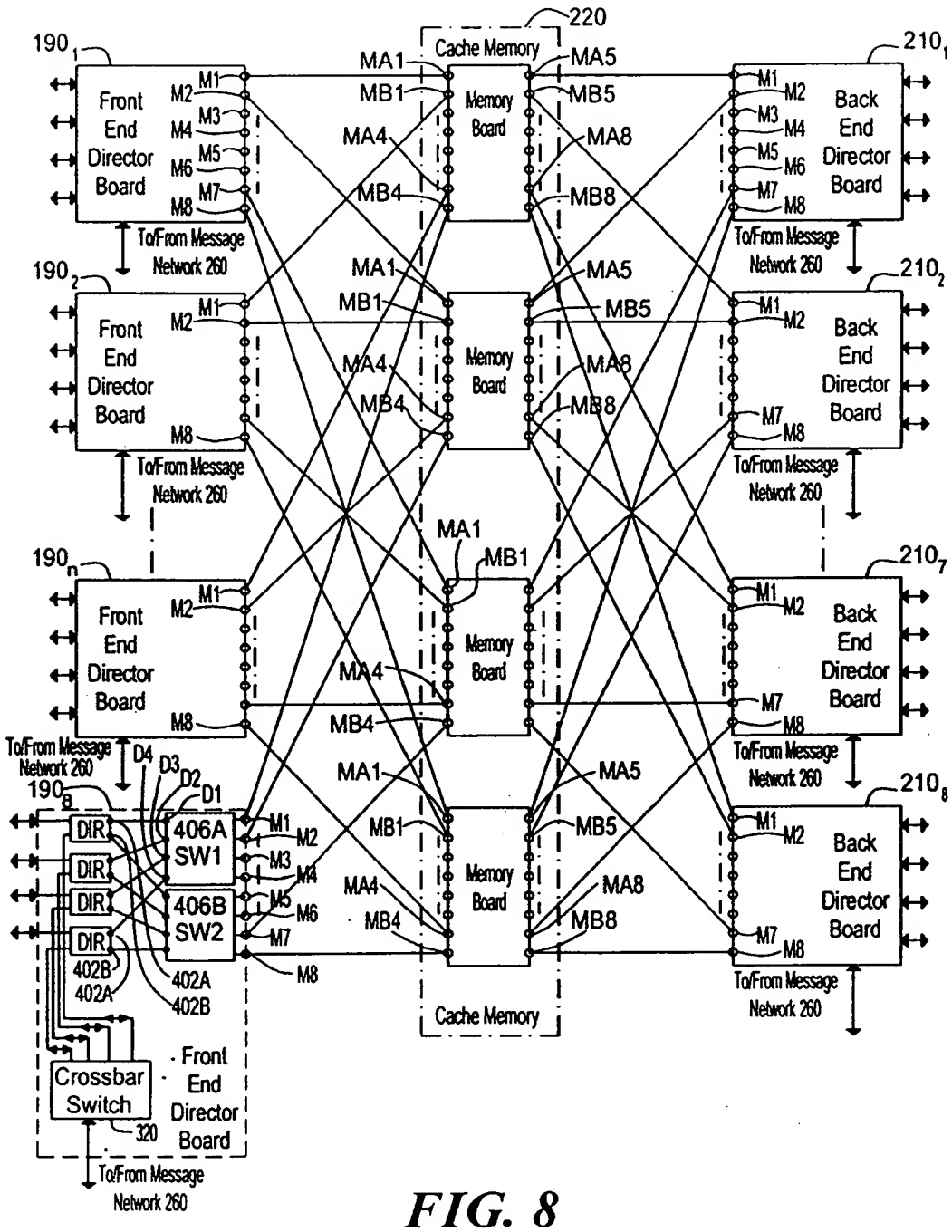
220
Cache Memory
190 1
190 2
190 n
190 8
Front End Director Board
To/From Message Network 260
Memory Board
MA1
MB1
MA4
MB4
MA5
MB5
MA8
MB8
M1
M2
M3
M4
M5
M6
M7
M8
210 1
210 2
210 7
210 8
Back End Director Board
DIR
406A SW1
406B SW2
D1
D2
D3
D4
402A
402B
Crossbar Switch
320
Front End Director Board
Cache Memory

FIG. 8

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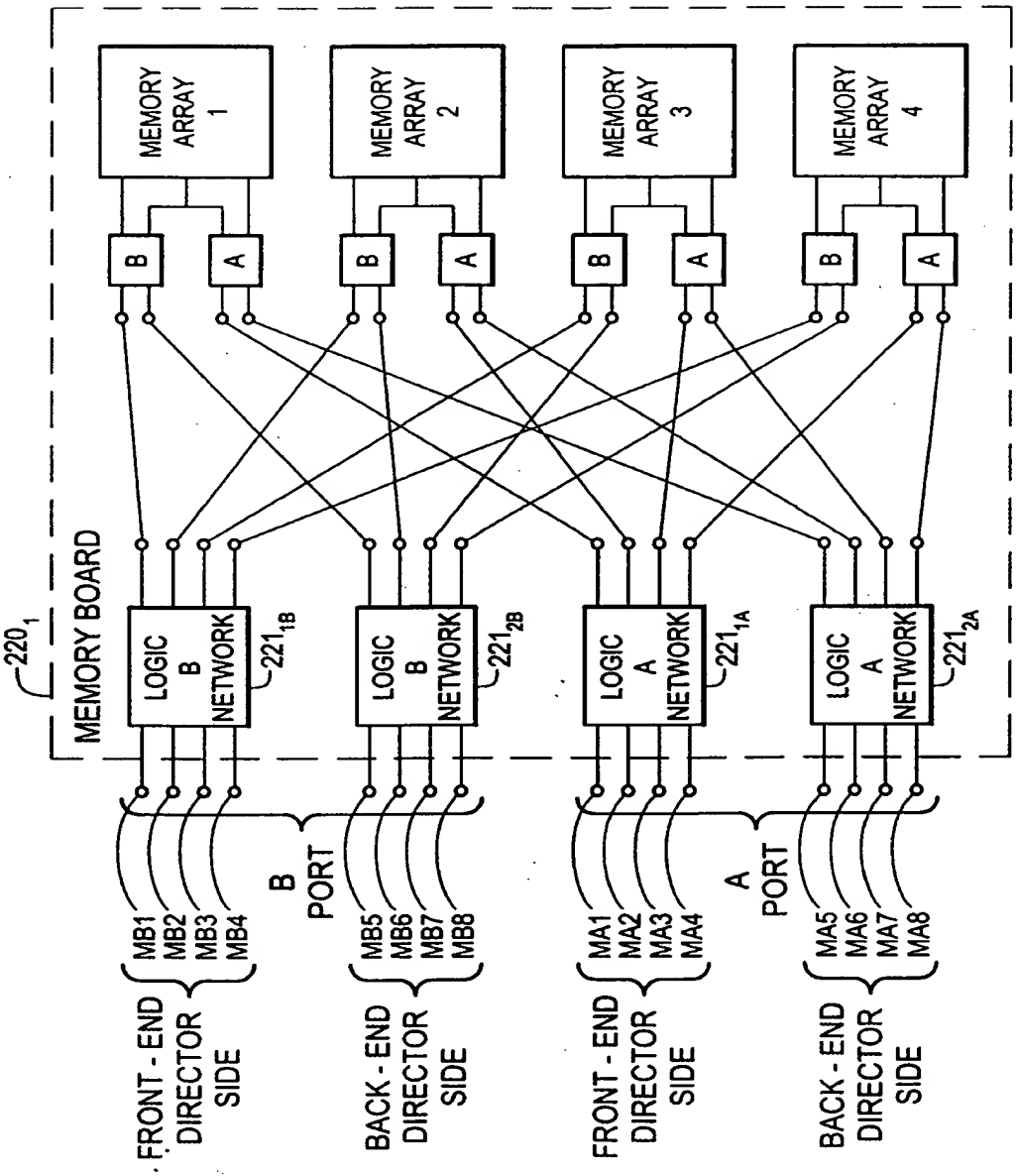
MEMORY BOARD
220 1
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
LOGIC B NETWORK
221 1B
LOGIC B NETWORK
221 2B
LOGIC A NETWORK
221 1A
LOGIC A NETWORK
221 2A
B PORT
A PORT
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
FRONT - END DIRECTOR SIDE
BACK - END DIRECTOR SIDE
FRONT - END DIRECTOR SIDE
BACK - END DIRECTOR SIDE

FIG. 8A

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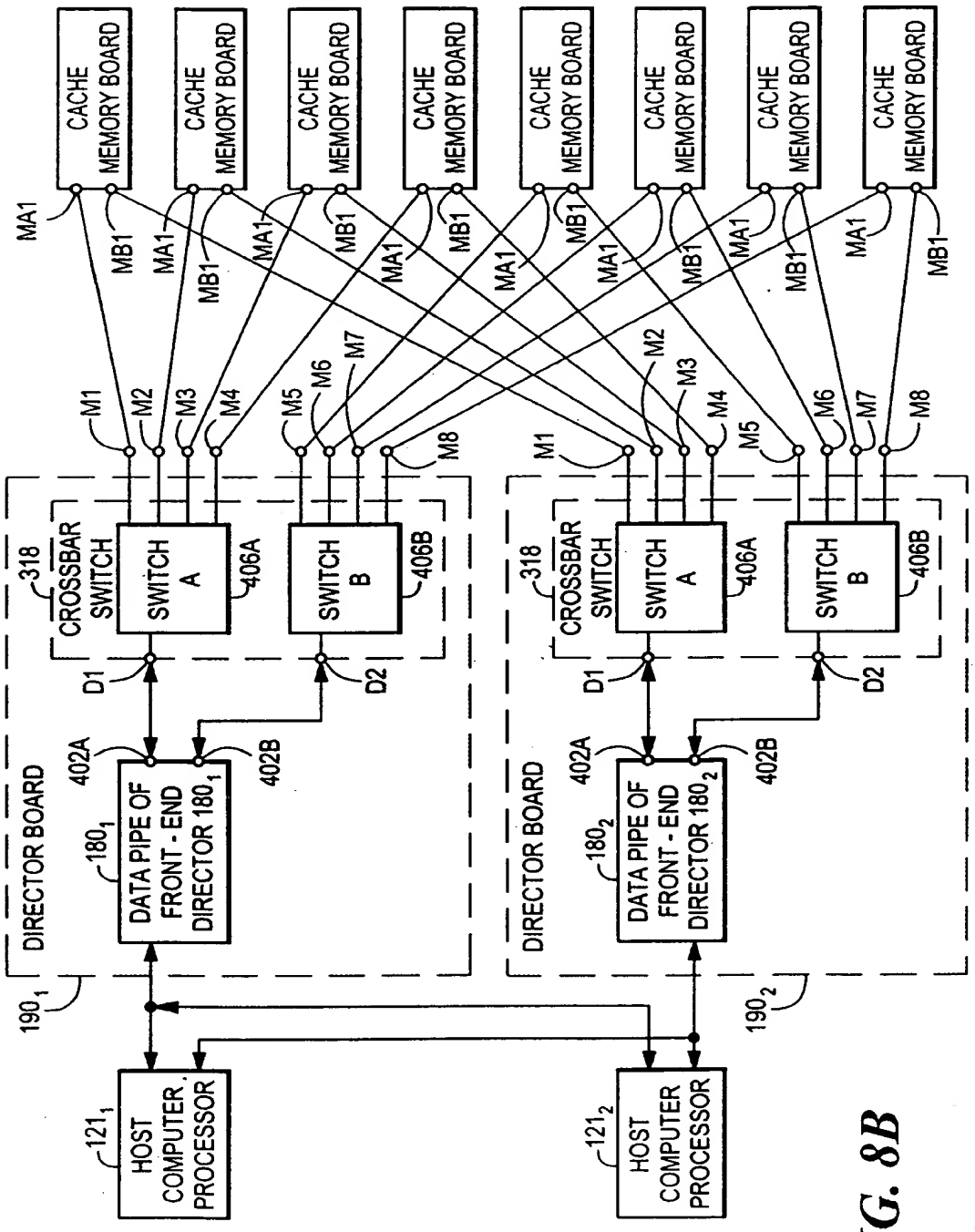
CACHE MEMORY BOARD
MA1
MB1
M1
M2
M3
M4
M5
M6
M7
M8
318
CROSSBAR SWITCH
SWITCH A
406A
SWITCH B
406B
D1
D2
402A
402B
DIRECTOR BOARD
DATA PIPE OF FRONT - END DIRECTOR 180
HOST COMPUTER PROCESSOR

FIG. 8B

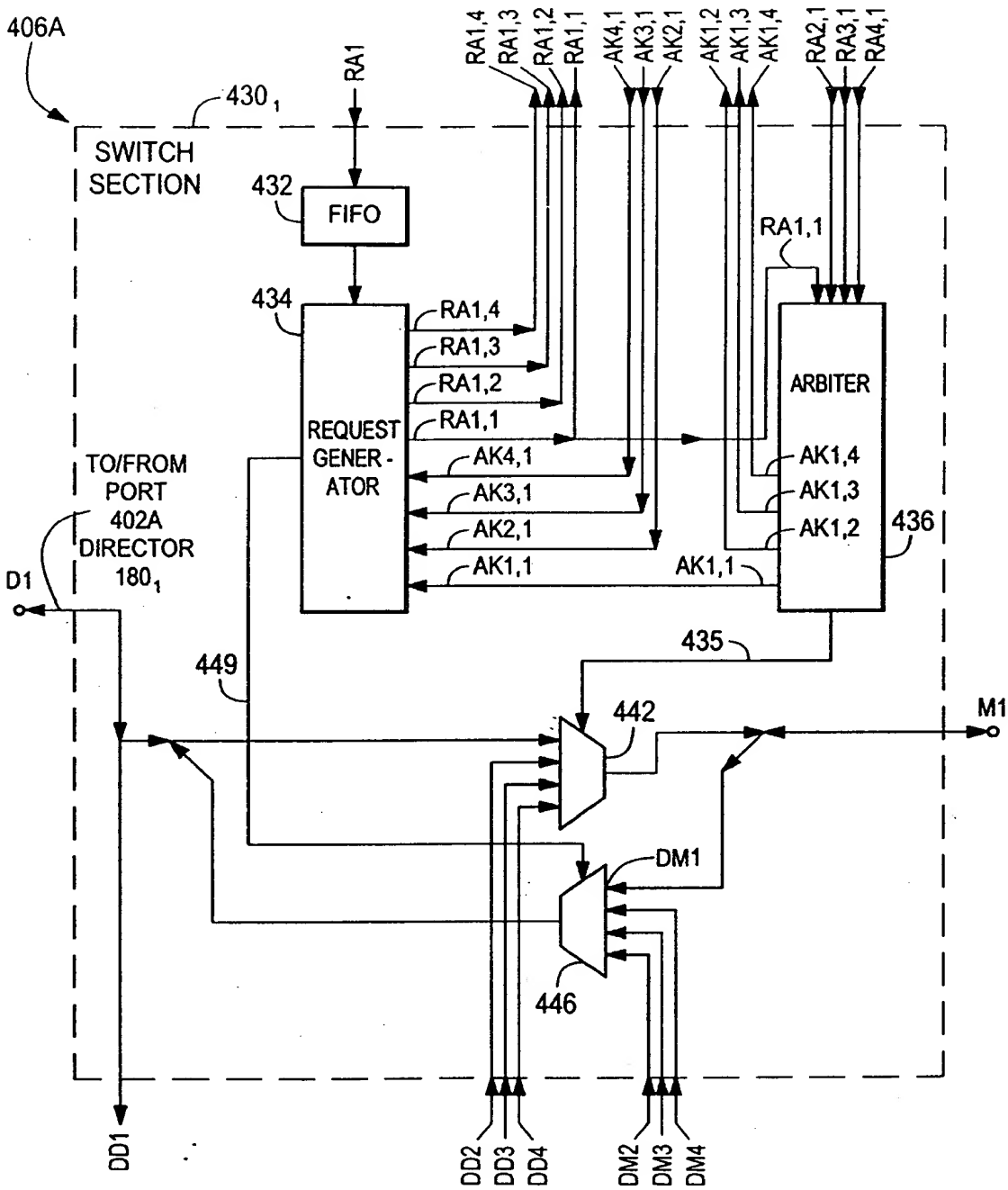

FIG. 8C-1

FIG. 8C

FIG. 8C-1
FIG. 8C-2

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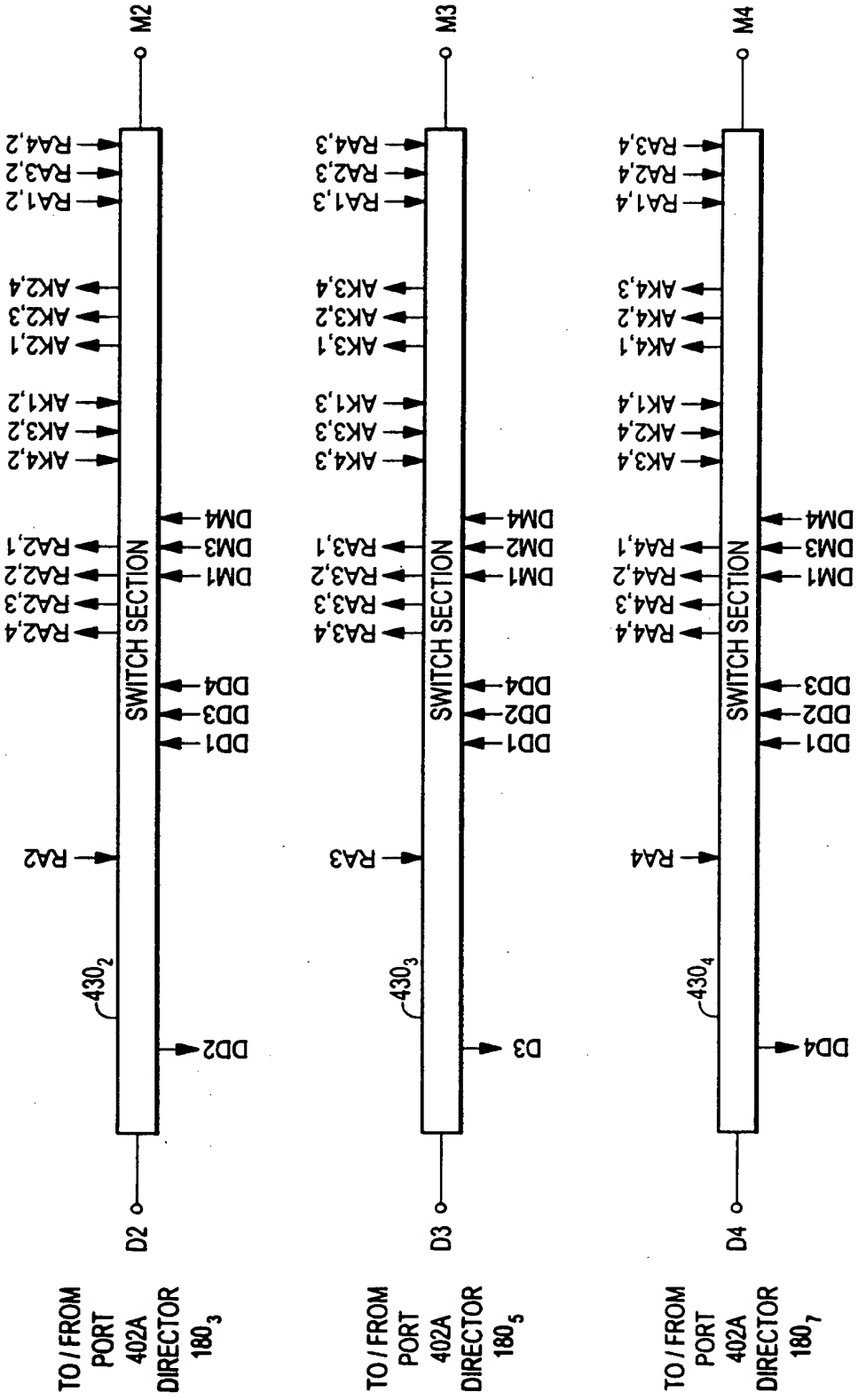
M2
M3
M4
RA4,2
RA3,2
RA1,2
AK2,4
AK2,3
AK2,1
AK1,2
AK3,2
AK4,2
DM4
DM3
DM1
RA2,1
RA2,2
RA2,3
RA2,4
DD4
DD3
DD1
RA2
430_2
DD2
SWITCH SECTION
D2
TO / FROM PORT 402A DIRECTOR 180_3
RA4,3
RA2,3
RA1,3
AK3,4
AK3,2
AK3,1
AK1,3
AK3,3
AK4,3
DM4
DM2
DM1
RA3,1
RA3,2
RA3,3
RA3,4
DD4
DD2
DD1
RA3
430_3
D3
SWITCH SECTION
D3
TO / FROM PORT 402A DIRECTOR 180_5
RA3,4
RA2,4
RA1,4
AK4,3
AK4,2
AK4,1
AK1,4
AK2,4
AK3,4
DM4
DM3
DM1
RA4,1
RA4,2
RA4,3
RA4,4
DD3
DD2
DD1
RA4
430_4
DD4
SWITCH SECTION
D4
TO / FROM PORT 402A DIRECTOR 180_7

FIG. 8C-2

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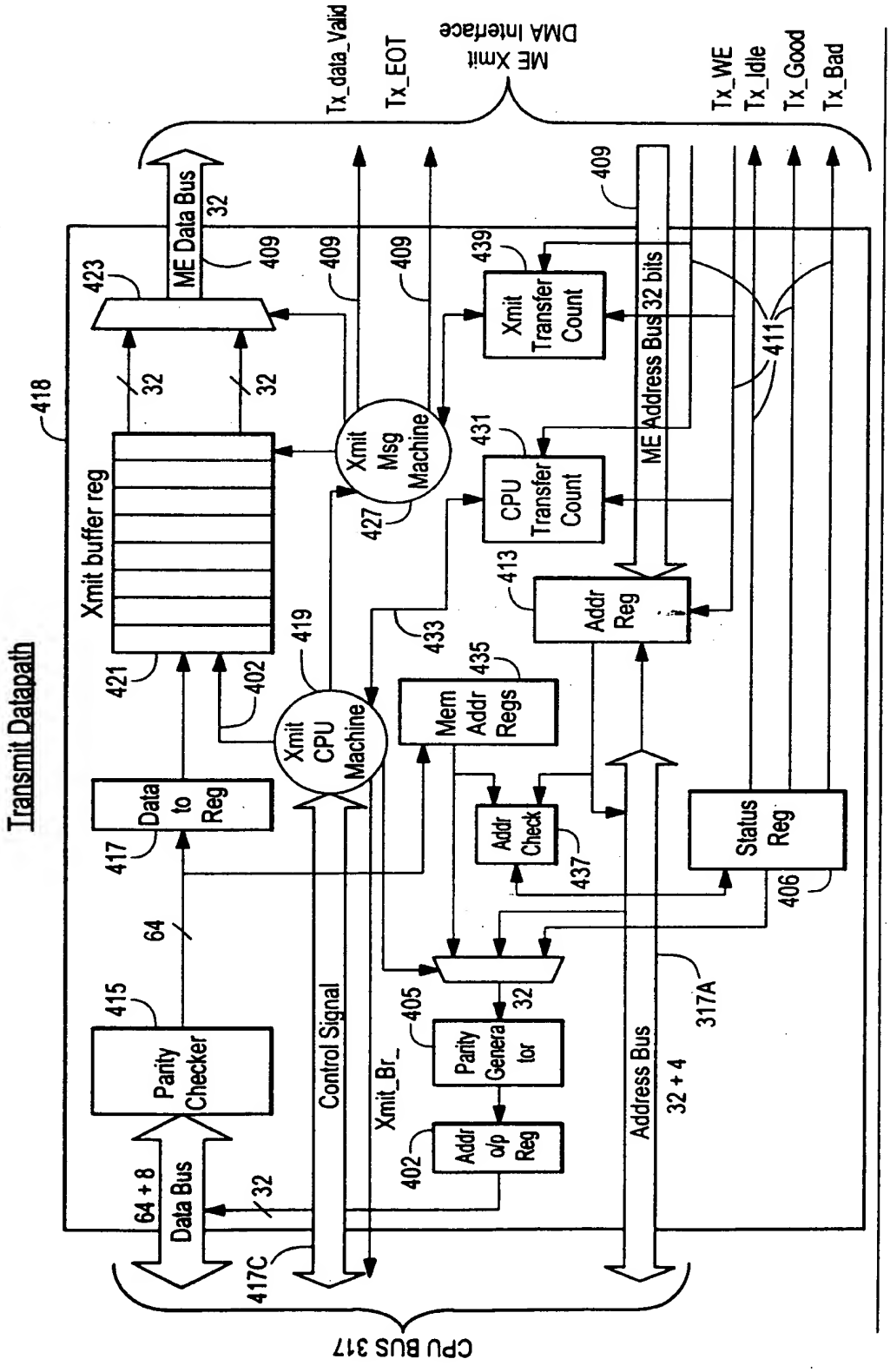
Transmit Datapath
Tx_data_Valid
Tx_EOT
ME Xmit DMA Interface
Tx_WE
Tx_Idle
Tx_Good
Tx_Bad
ME Data Bus
32
ME Address Bus 32 bits
Xmit buffer reg
Xmit Msg Machine
Xmit Transfer Count
CPU Transfer Count
Addr Reg
Xmit CPU Machine
Mem Addr Regs
Addr Check
Status Reg
Data to Reg
Parity Checker
Parity Genera tor
Addr o/p Reg
64 + 8 Data Bus
Control Signal
Xmit_Br_
Address Bus
32 + 4
CPU BUS 317
418
423
409
439
411
431
427
413
433
419
435
421
402
417
64
415
405
317A
406
437
417C

FIG. 9

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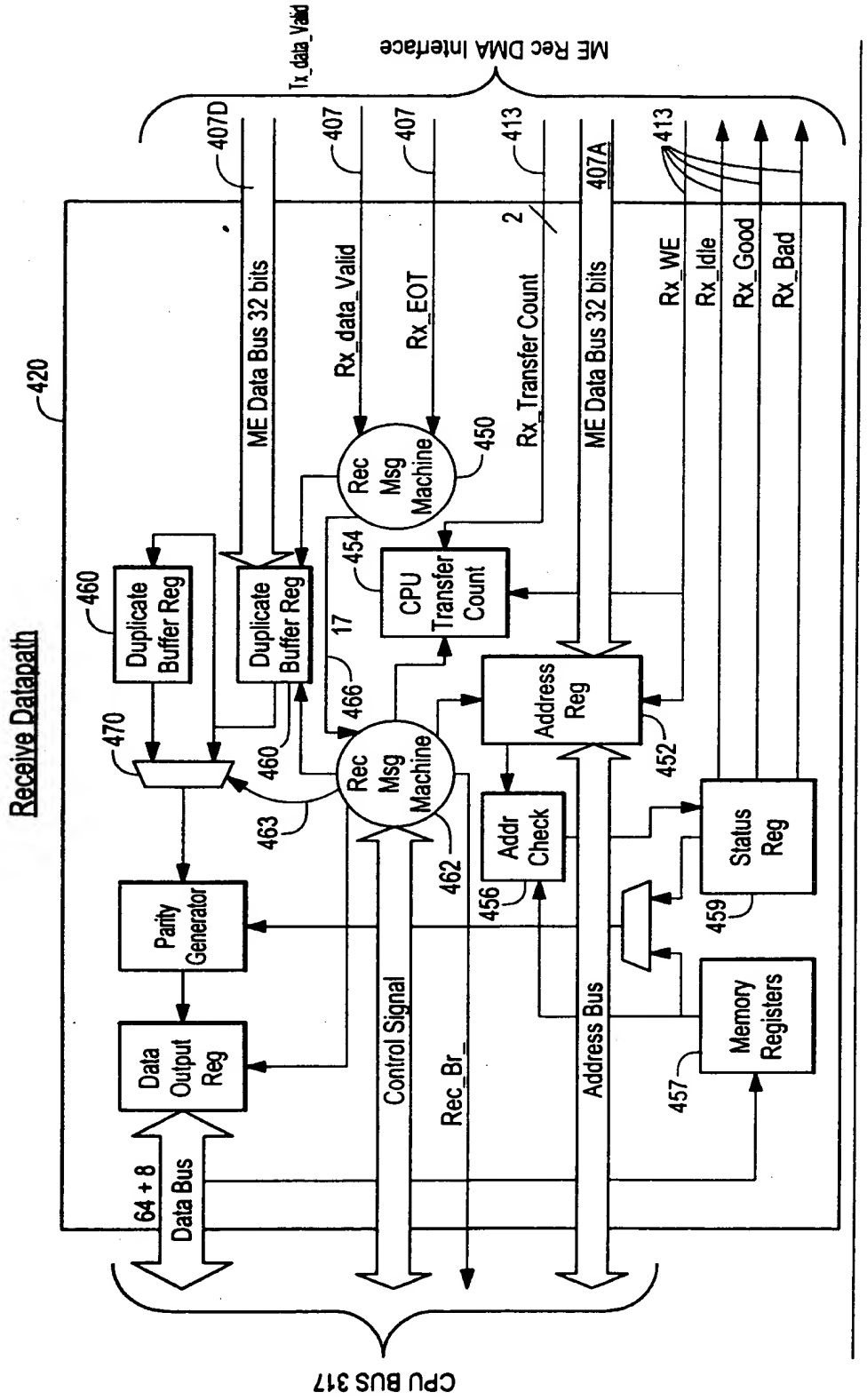
ME Rec DMA Interface
Tx_data_Valid
407D
407
407
413
407A
413
420
ME Data Bus 32 bits
Rx_data_Valid
Rx_EOT
2
Rx_Transfer Count
ME Data Bus 32 bits
Rx_WE
Rx_Idle
Rx_Good
Rx_Bad
Receive Datapath
Rec Msg Machine
450
454
CPU Transfer Count
460
Duplicate Buffer Reg
Duplicate Buffer Reg
17
466
Address Reg
470
460
Rec Msg Machine
452
463
462
Addr Check
456
Status Reg
459
Parity Generator
Data Output Reg
Control Signal
Rec_Br_
Address Bus
Memory Registers
457
64 + 8 Data Bus
CPU BUS 317

FIG. 10

FIG. 11

FIG. 11A

FIG. 11B

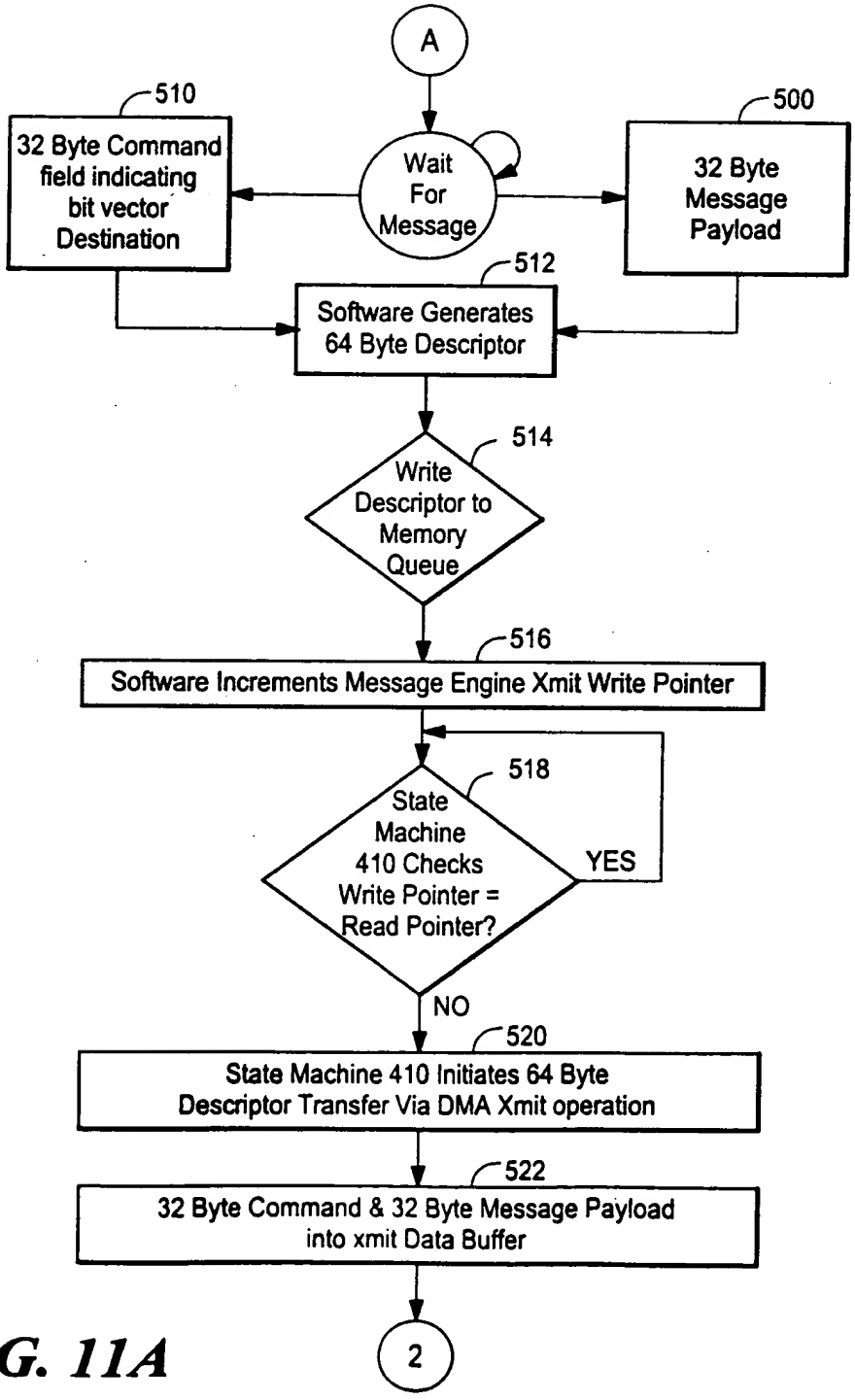

FIG. 11A

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Message Bus Send Operation Continued

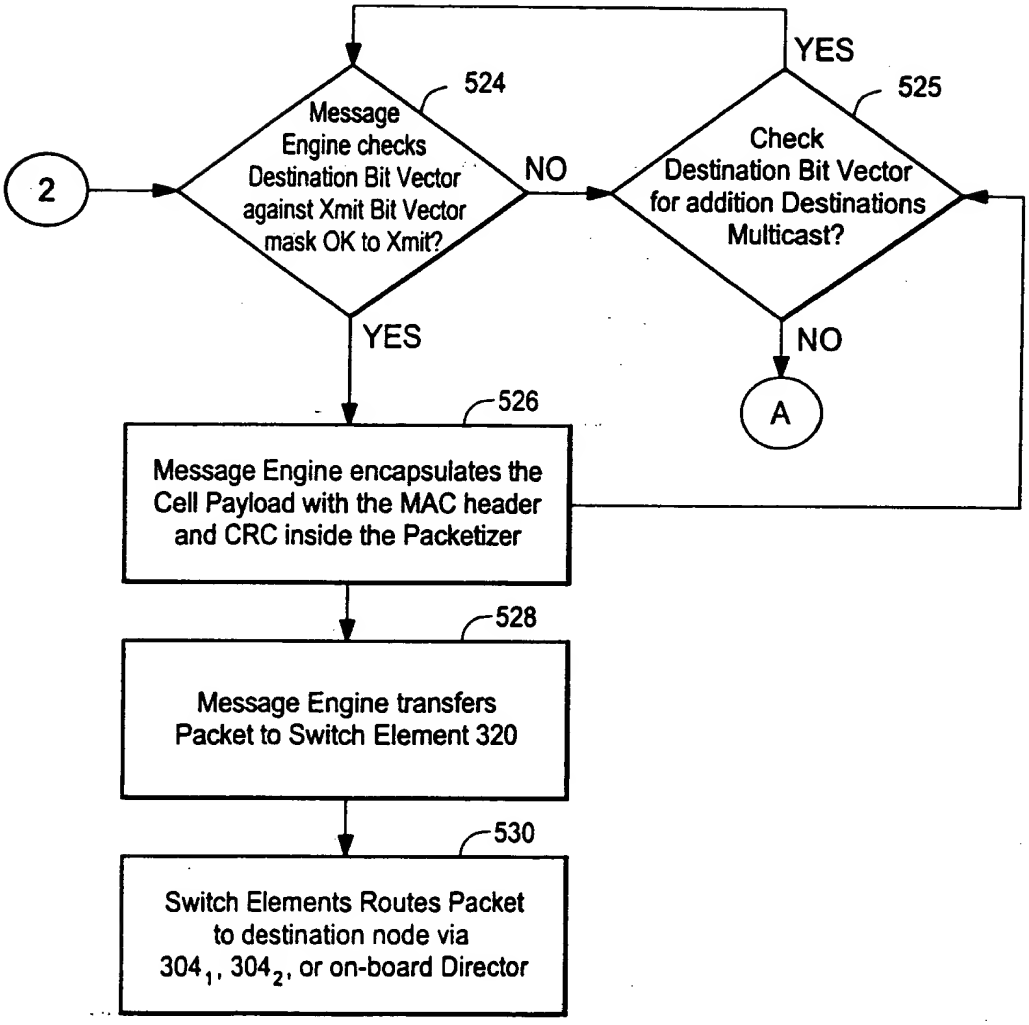

FIG. 11B

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FIG. 11C

FIG. 11D

FIG. 11E

FIG. 11F

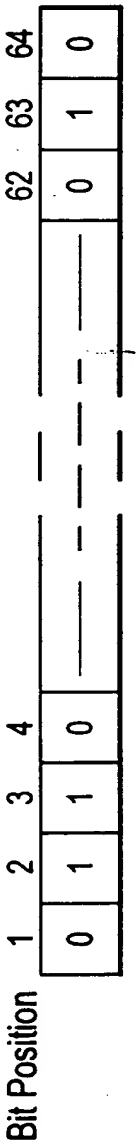

FIG. 11G

FIG. 12

FIG. 12A

FIG. 12B

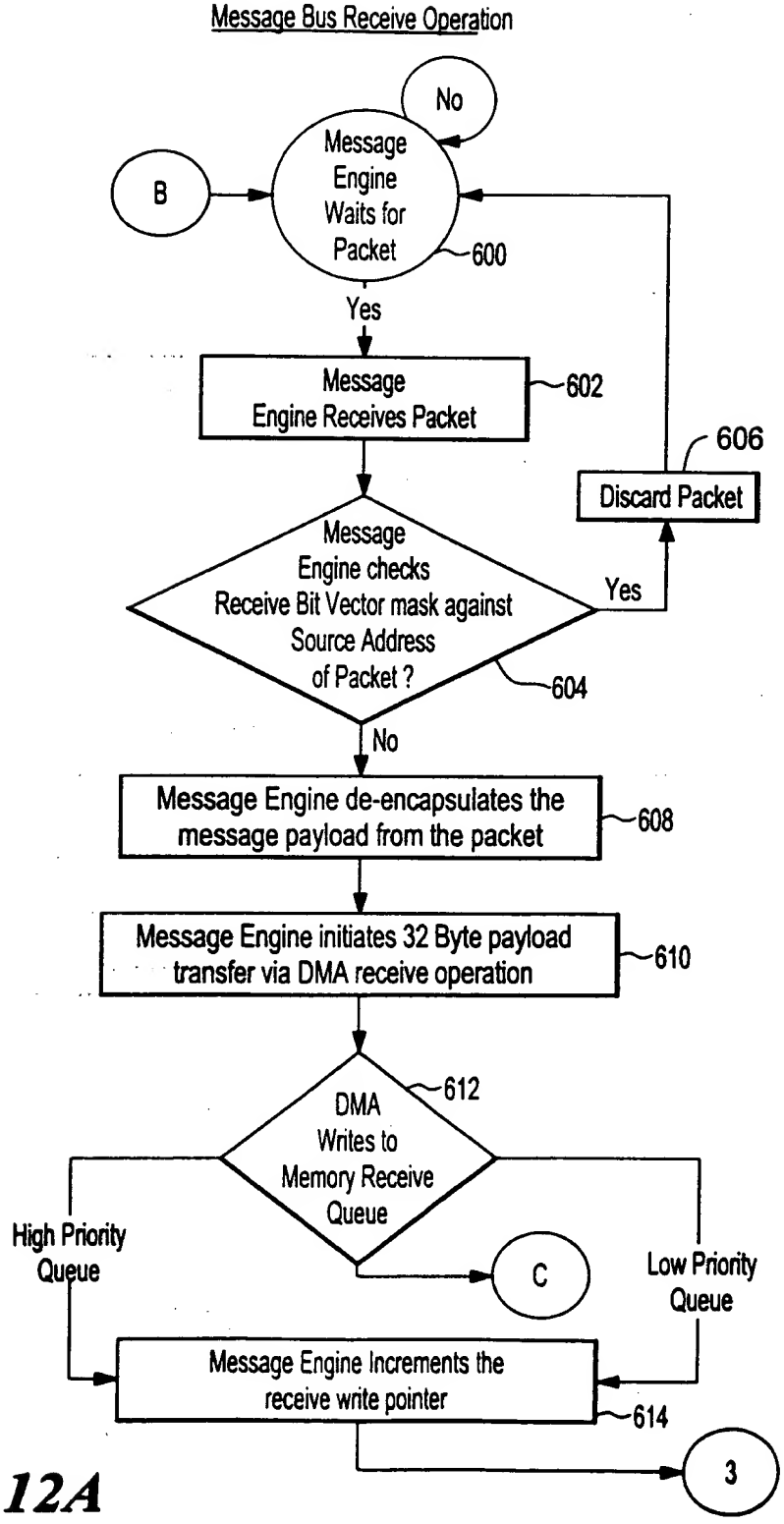

FIG. 12A

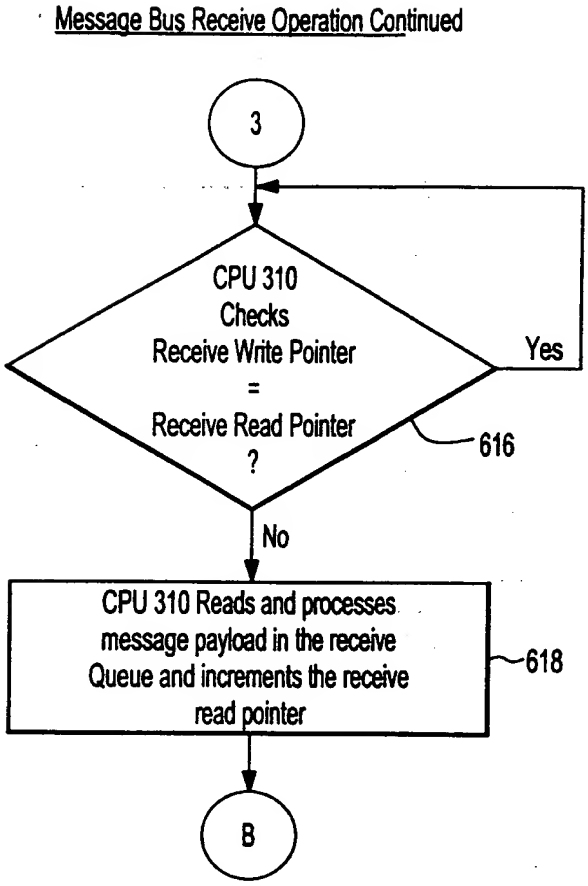
Message Bus Receive Operation Continued
3
CPU 310
Checks
Receive Write Pointer
=
Receive Read Pointer
?
Yes
616
No
CPU 310 Reads and processes
message payload in the receive
Queue and increments the receive
read pointer
618
B

FIG. 12B

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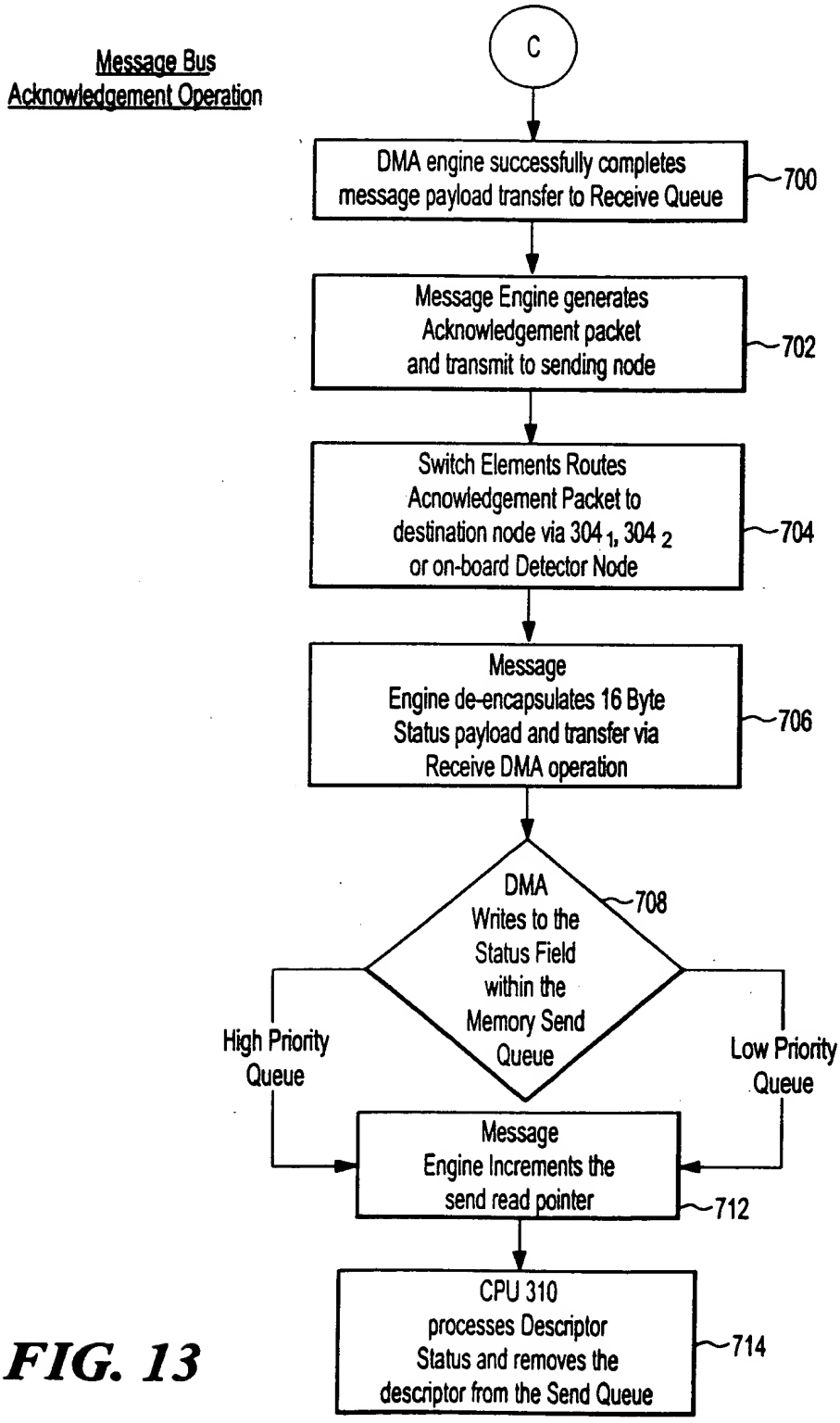
Message Bus
Acknowledgement Operation
C
DMA engine successfully completes message payload transfer to Receive Queue
700
Message Engine generates Acknowledgement packet and transmit to sending node
702
Switch Elements Routes Acnowledgement Packet to destination node via 304 1, 304 2 or on-board Detector Node
704
Message Engine de-encapsulates 16 Byte Status payload and transfer via Receive DMA operation
706
DMA Writes to the Status Field within the Memory Send Queue
708
High Priority Queue
Low Priority Queue
Message Engine Increments the send read pointer
712
CPU 310 processes Descriptor Status and removes the descriptor from the Send Queue
714

FIG. 13

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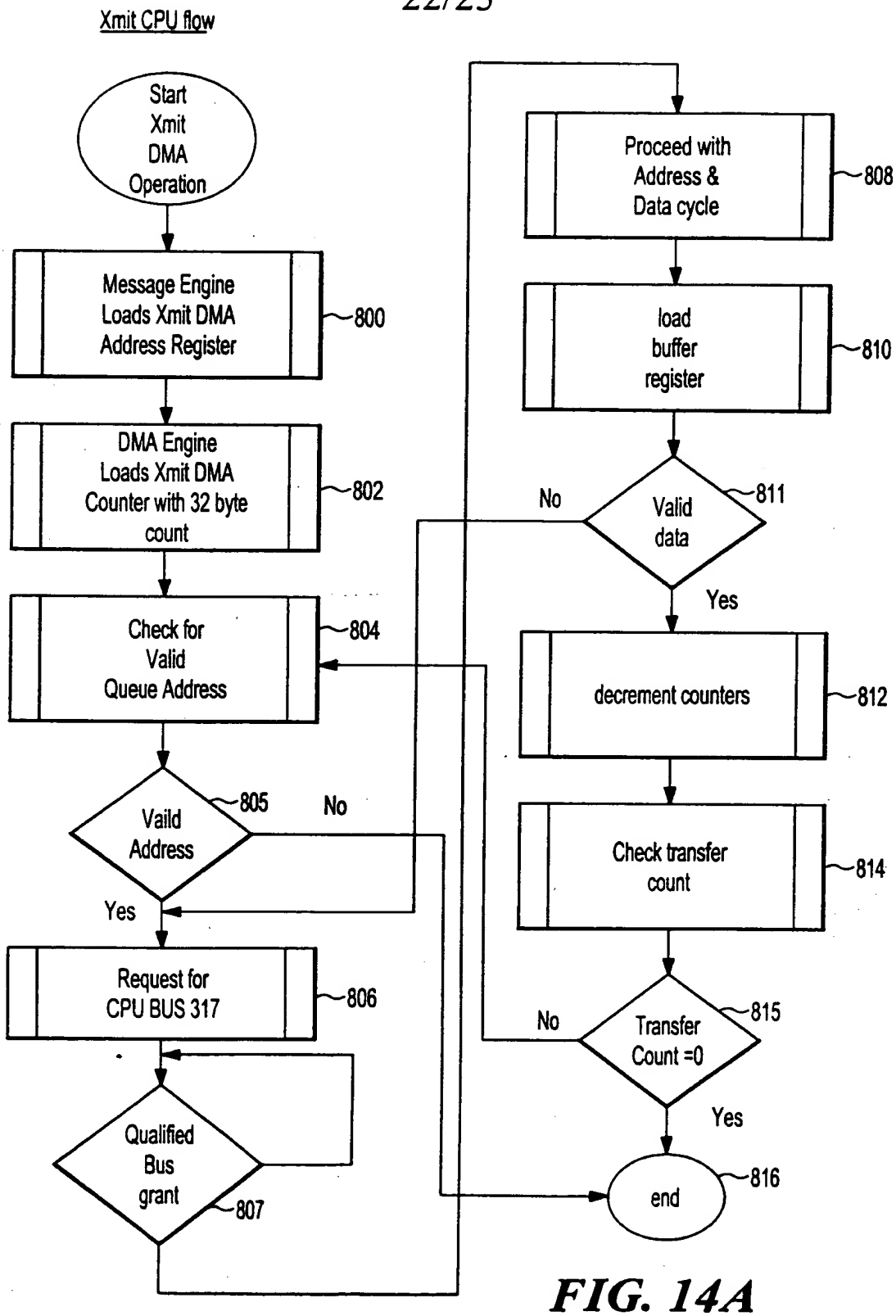
Xmit CPU flow
Start Xmit DMA Operation
Message Engine Loads Xmit DMA Address Register
800
DMA Engine Loads Xmit DMA Counter with 32 byte count
802
Check for Valid Queue Address
804
Vaild Address
805
No
Yes
Request for CPU BUS 317
806
Qualified Bus grant
807
Proceed with Address & Data cycle
808
load buffer register
810
Valid data
811
No
Yes
decrement counters
812
Check transfer count
814
Transfer Count =0
815
No
Yes
end
816

FIG. 14A

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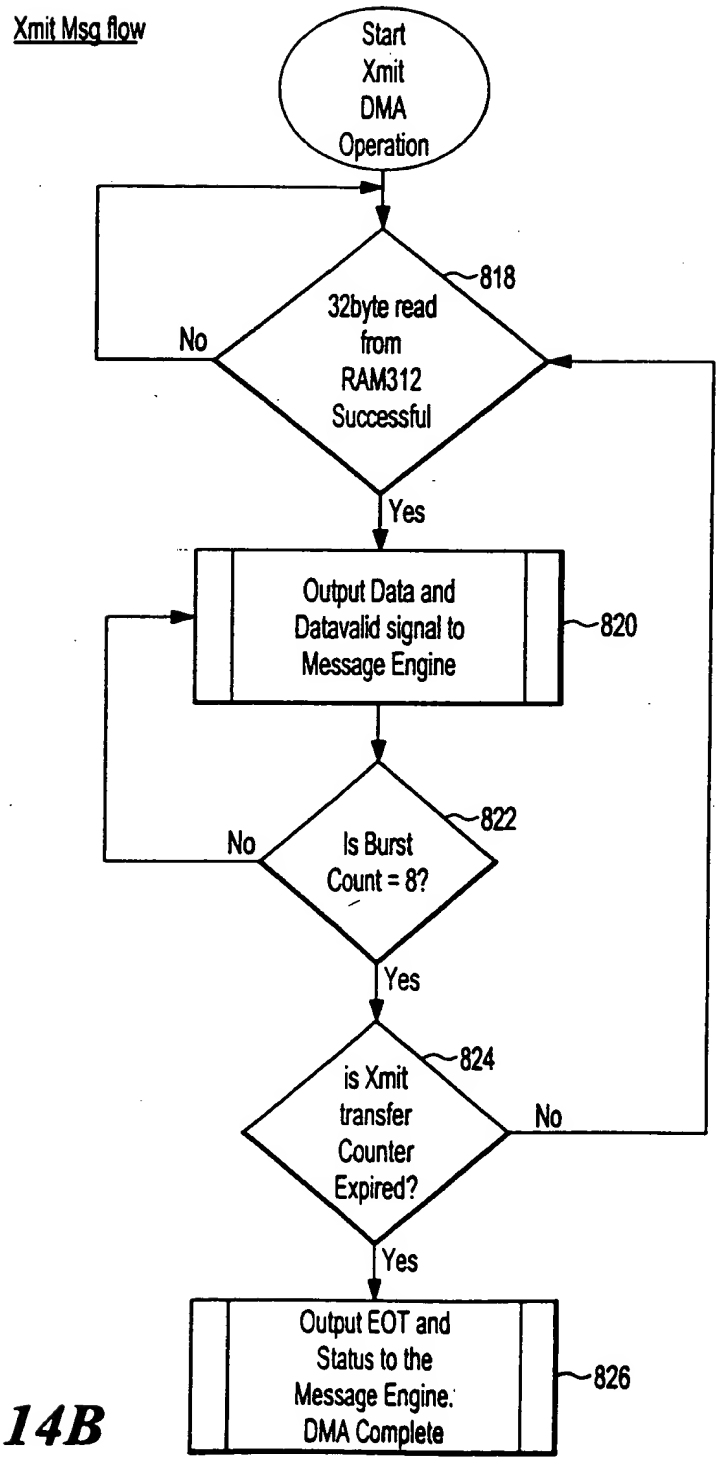
Xmit Msg flow
Start Xmit DMA Operation
818
32byte read from RAM312 Successful
No
Yes
Output Data and Datavalid signal to Message Engine
820
822
Is Burst Count = 8?
No
Yes
824
is Xmit transfer Counter Expired?
No
Yes
Output EOT and Status to the Message Engine. DMA Complete
826

FIG. 14B

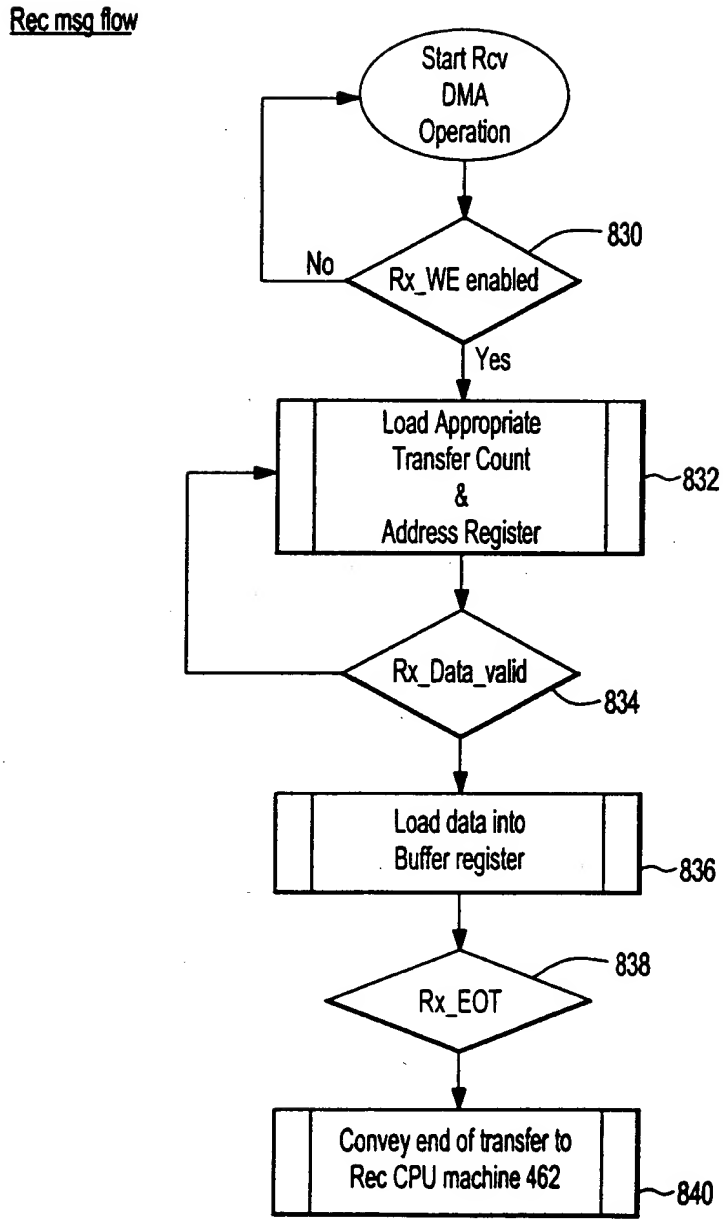
Rec msg flow
Start Rcv DMA Operation
830
No
Rx_WE enabled
Yes
Load Appropriate Transfer Count & Address Register
832
Rx_Data_valid
834
Load data into Buffer register
836
838
Rx_EOT
Convey end of transfer to Rec CPU machine 462
840

FIG. 15A

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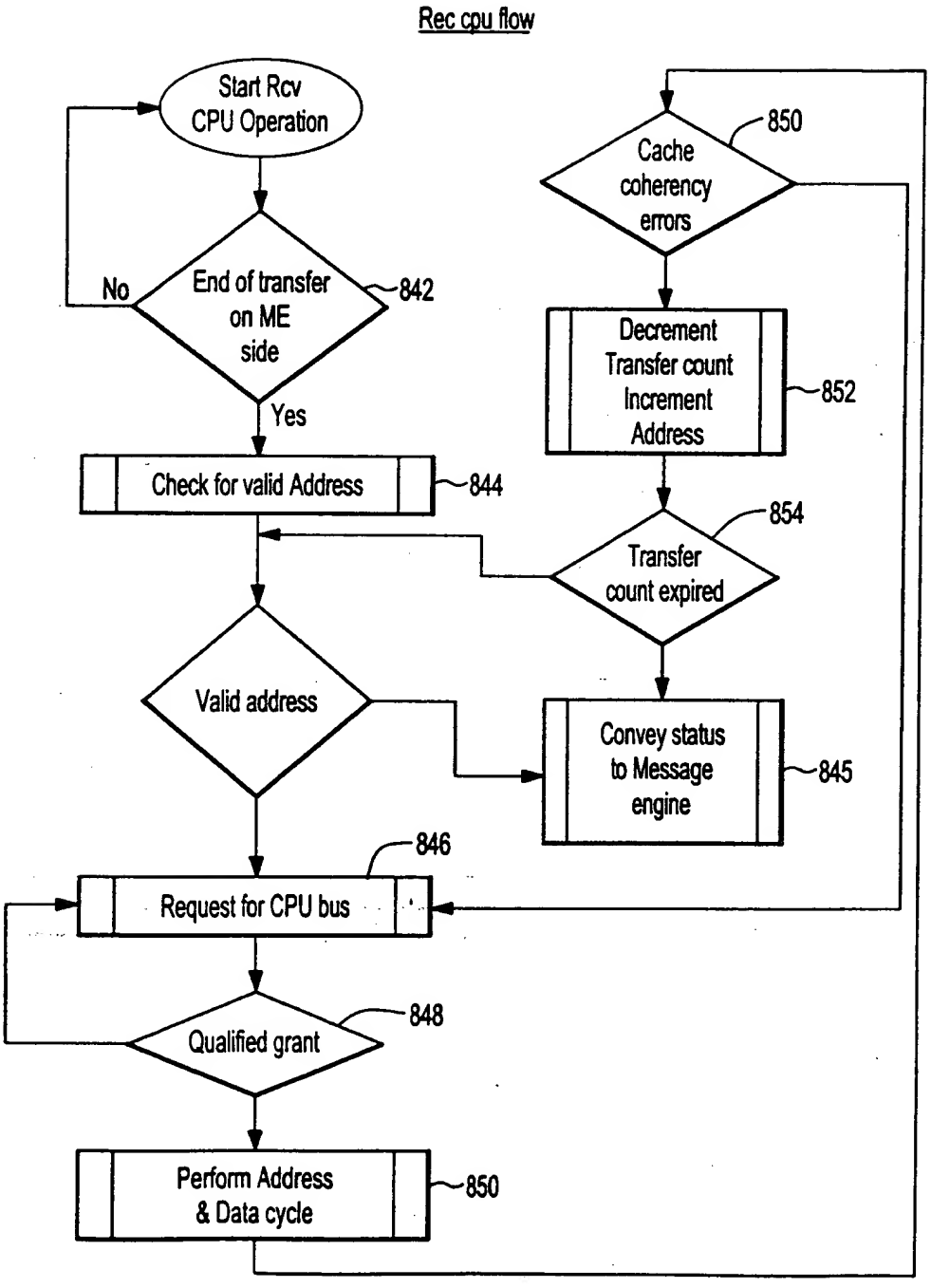
Rec cpu flow
Start Rcv CPU Operation
End of transfer on ME side
No
Yes
842
Check for valid Address
844
Valid address
Request for CPU bus
846
Qualified grant
848
Perform Address & Data cycle
850
Cache coherency errors
850
Decrement Transfer count Increment Address
852
Transfer count expired
854
Convey status to Message engine
845

FIG. 15B